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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,661	10/30/2007	Peter Deixler	US030427US2	9703

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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
07/08/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,661	DEIXLER ET AL.	
	Examiner	Art Unit	
	RON POMPEY	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Knoll** et al. (US 7205188) in view of **Voldman** (US 6465870).

Knoll discloses the limitations of:

In re claim 1: A method of fabricating an integrated circuit, the method comprising: providing a substrate (0, fig. 1a), creating at least one base-window (opening in 4, will etch 2/3, fig. 1a (not shown)) in a layer to expose a surface of the substrate; forming a monocrystalline SiGe layer in at least one region (6/6a/6b, fig. 1b) of the base-window, and forming a polycrystalline SiGe layer (7, fig. 1b) elsewhere over the substrate.

In re claim 2: A method as recited in claim 1, further comprising forming a polycrystalline silicon layer (12, fig. 1d) over selectively exposed portions of the substrate.

In re claim 3: A method as recited in claim 2, further comprising forming a mask (10, fig. 1c) over a top surface, providing openings in selected locations of the mask,

and removing the polycrystalline silicon layer (9, fig. 1c) to expose the selected portions of the substrate.

In re claim 4: A method as recited in claim 3, wherein the exposed portions of the substrate are monocrystalline silicon (0 (substrate is monocrystalline), fig. 1c).

In re claim 5: A method as recited in claim 1, wherein the integrated circuit includes a lateral pnp transistor (33a, 33b, 33c, fig. 1p).

In re claim 6: A method as recited in claim 1, wherein the integrated circuit includes a SiGe bipolar transistor (SiGe-HBT, col. 4, lns. 27-30).

In re claim 7: A method as recited in claim 6, wherein the SiGe bipolar transistor includes the monocrystalline SiGe (col.4, lns. 20-28).

2. However, **Knoll does not disclose** forming a monocrystalline SiGe layer on the exposed surface of the substrate.

a. **Voldman** discloses:

forming a monocrystalline SiGe layer on the exposed surface of the substrate (col. 4, lns. 45-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the number of layers used to form the base layer of Knoll, with the single monocrystalline SiGe layer on the exposed substrate as taught by Voldman, because using one layer instead of multiple layers will reduce production time and cost of making the device.

3. Claim 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knoll in view of Voldman as applied to claim 1 above, in view of APA(admitted prior art).

4. Knoll, as indicated above, discloses all the features of the claims **except:**

In re claim 8: A method as recited in claim 1, wherein the integrated circuit includes a varactor diode.

In re claim 9: A method as recited in claim 1, further comprising forming a polysilicon resistor.

In re claim 10: A method as recited in claim 1, wherein only one masking step is required to form a lateral pnp transistor, varactor diode and a polysilicon resistor.

In re claim 11: A method as recited in claim 10, wherein the lateral pnp transistor is a silicon device, and includes a portion of the polycrystalline SiGe layer in each of a collector contact and an emitter contact.

In re claim 12: A method as recited in claim 11, wherein the polycrystalline SiGe layer is disposed beneath a polycrystalline silicon layer.

b. However, **APA** discloses:

In re claim 8: A method as recited in claim 1, wherein the integrated circuit includes a varactor diode (page 1, lns. 9-25).

In re claim 9: A method as recited in claim 1, further comprising forming a polysilicon resistor (page 1, lns. 6-8).

In re claim 10: A method as recited in claim 1, wherein only one masking step is required to form a lateral pnp transistor, varactor diode and a polysilicon resistor (page 1, lns. 17-19).

In re claim 11: A method as recited in claim 10, wherein the lateral pnp transistor is a silicon device, and includes a portion of the polycrystalline SiGe layer in each of a collector contact and an emitter contact (page 1, lns. 1-32 (APA); the polycrystalline SiGe in 33a, fig. 1p of Knoll).

In re claim 12: A method as recited in claim 11, wherein the polycrystalline SiGe layer is disposed beneath a polycrystalline silicon layer (12, fig. 1d; Knoll).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the integrated circuit in **Knoll and Voldman**, with the lateral pnp transistor, varactor diode and a polysilicon resistor as taught by **APA**, because Knoll is silent in including a lateral pnp transistor, varactor diode and a polysilicon resistor in its BiCMOS device and these other components, lateral pnp transistor, varactor diode and a polysilicon resistor, will make Knoll's BiCMOS device more robust.

Response to Arguments

2. Applicant's arguments with respect to claims 1-12, received 3/29/10, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RON POMPEY whose telephone number is (571)272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

/R. P./
Examiner, Art Unit 2812
07/03/10